Hsu fails to teach or suggest controlling a parameter of deposition of metal layer 430 (or any other metal deposition parameter) such that metal layer 430 (or another deposited metal layer) has a predetermined property that causes subsequent reaction of the metal with silicon (to form metal salicide regions) to occur in a source limited manner and limits metal (e.g., cobalt) salicide crawl during formation of the metal salicide regions (as recited in claims 1 and 8), or depositing a metal layer having a predetermined thickness over an IC structure, then removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed, and then reacting remaining portions of the metal layer with silicon of the MOS transistor structures to form metal salicide regions in a source limited manner (as recited in claim 13). The Examiner has not contended that Hsu includes such a teaching or suggestion.

By controlling a predetermined property (e.g., thickness) of deposited metal in accordance with the invention, a metal salicide formation reaction (also referred to herein as a salicidation or silicidation reaction) can be driven to completion in the sense that the reaction is allowed to continue until a limited amount of metal (available for reaction) is consumed by the reaction. The inventive salicidation reaction can thus be "source limited" in the sense that it is limited by the amount of metal available for reaction.

Rather than teaching or suggesting the claimed invention, Hsu teaches away from the invention by teaching a conventional method in which more metal 430 is deposited (and allowed to remain available for reaction) than will react during a subsequent salicide-forming reaction. Specifically, Hsu teaches at col. 6, line 65-col. 7, line 5, that unreacted metal 430 is removed (e.g., by dry etching) from over structures 410, 412, 414, 420 and 423 after a salicide-forming reaction, leaving salicide layers 450 exposed (as shown in Fig. 3F). Hsu's salicide layers 450 are not formed in a source limited manner, since metal over structures 416 (which are salicide exclusion regions) is available for forming salicide layers 450 and since there is more metal over structures 410, 412, 420, and 423 available for forming salicide than is actually used for forming salicide layers 450.

Goto also fails to teach formation of metal salicide regions in a source limited manner as recited in claims 1, 8, and 13. Goto fails to teach or suggest controlling a metal deposition

parameter such that a deposited metal layer has a predetermined property that causes subsequent reaction of the metal with silicon (to form metal salicide regions) to occur in a source limited manner and limits metal (e.g., cobalt) salicide crawl during formation of the metal salicide regions (as recited in claims 1 and 8), or depositing a metal layer having a predetermined thickness over an IC structure, then removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed, and then reacting remaining portions of the metal layer with silicon of the MOS transistor structures to form metal salicide regions in a source limited manner (as recited in claim 13).

Goto teaches depositing metal (e.g., cobalt layer 11 Fig. 1D), and titanium nitride (TiN layer 12 of Fig. 1D) over the metal, over all regions of a semiconductor structure. A silicidation reaction is then performed before any of the metal is removed from over any portion of the structure where a salicide exclusion region is to be formed (in contrast with the method of claim 1, 8, or 13). Goto teaches at col. 9, lines 5-12, that metal salicide (e.g., salicide 11g, 11d, and 11s of Fig. 1E) is formed under the overlying titanium nitride layer, as shown in Fig. 1E. Then, as described at col. 9, lines 13-20, the titanium nitride (12) is removed and the unreacted metal (11) is then removed to produce a structure with exposed metal salicide (the structure shown in Fig. 1F). Then, an annealing operation is performed to lower the resistance of the metal salicide. If Goto's silicidation reaction were source limited, Goto would not need to remove residual (unreacted) metal from the vicinity of Goto's metal salicide regions after Goto's salicidation reaction, as described in Goto with reference to Figs. 1E and 1F.

To form the structure shown in Goto's Fig. 7A, Goto teaches (at col. 6) performance of operations similar to those described in Goto with reference Figs. 1D, 1E, and 1F. A continuous layer of metal (e.g., titanium or cobalt) is deposited over all regions of a semiconductor structure. A silicidation reaction (including two annealing stages) is then performed before any of the metal is removed from over any portion of the structure where a salicide exclusion region is to be formed (in contrast with the method of claim 1, 8, or 13). Then, as described at col. 6, lines 47-48, the unreacted metal is removed to produce the Fig. 7A structure which has exposed metal silicide 58.

The Examiner has cited Goto's teaching (at col. 6, lines 41-42) that during formation of Goto's Fig. 7A structure, a "predetermined thickness" (T) of metal is deposited during a pre-reaction metal deposition step. However, this is not a teaching to control deposited metal thickness so as to achieve a source limited reaction (in which all metal present at the start of the reaction reacts), and does not amount to a teaching or suggestion to modify Hsu's method to reach the invention of claim 1, 8, or 13.

Goto teaches control of the thickness of a deposited metal layer for the purpose of affecting the sheet resistance of metal salicide formed by a silicidation reaction and subsequent annealing. See, for example, Goto's teaching at col. 10, line 50- col. 11, line 8 (with reference to Fig. 6A). Goto teaches at col. 10, line 59 to col. 11, line 4, that a sufficiently thick metal layer (thicker than 5 nm) should be used to achieve a desirably low metal salicide sheet resistance, since use of a thinner metal layer (thinner than 5 nm) would result in a higher metal salicide sheet resistance.

Goto also teaches at col. 10, lines 45-50, that deposition of a metal layer that is too thick (i.e., a metal layer having thickness greater than 15 nm, where gate length is 0.3 μm or less) can (during subsequent salicidation of the metal) result in "destruction" of semiconductor junctions that are intended to underlie metal salicide to be formed during the salicidation reaction. Applicant believes this cannot reasonably be construed as a teaching to perform the salicidation reaction in a source limited manner.

Goto's teaching does not amount to a teaching or suggestion to modify Hsu's method to reach the invention of claim 1, 8, or 13. Not only does Goto fail to teach or suggest depositing metal with a predetermined thickness to achieve a source limited silicidation reaction, but Goto teaches away from the invention by teaching silicidation reactions that are not source limited. At above-cited col. 9, lines 13-20, Goto teaches a method in which metal 11 is deposited (presumably with a predetermined thickness), a silicidation reaction is then performed to produce metal salicide regions 11s, 11d, and 11g (shown in Goto's Figs. 1E and 1F), and unreacted metal 11 is then removed to produce a structure with exposed metal salicide (the structure shown in Fig. 1F). Because unreacted metal 11 is removed after the reaction, the reaction is not source limited. Similarly, at col. 6, lines 42-48, Goto teaches a

method in which metal is deposited, a silicidation reaction is then performed to produce metal silicide electrodes 58 (of Fig. 7A), and unreacted metal is then removed from the structure. Because unreacted metal is removed after the reaction, the reaction is not source limited.

When performing the conventional metal salicide formation methods described in Goto, there is an effectively unlimited supply of metal available for forming metal salicide. There is no teaching or suggestion determinable from Goto to perform a metal salicide forming reaction in a source limited manner. Nor is there any teaching or suggestion determinable from Goto that metal (e.g., metal remaining after a pre-silicidation reaction metal removal step) available to form metal salicide regions should have a predetermined property (e.g., thickness) that causes a metal salicide forming reaction to occur in a source limited manner. Goto instead teaches away from the claimed invention in the manner explained above.

Goto also fails to teach formation of metal salicide regions in a manner that limits metal (e.g. cobalt) salicide crawl, as recited in claims 1 and 8. The Examiner acknowledges that Goto "does not disclose reducing salicide crawl." However, the Examiner argues that the structure of Goto's Fig. 7A exhibits "no salicide crawl ... beyond the portions of the MOS transistor structure where metal salicide regions are to be formed." Applicant respectfully contends that the lack of apparent salicide crawl in Fig. 7A in no way implies that no such salicide crawl would result from implementing Goto's explicit teachings. There is no teaching or suggestion determinable from Goto that Fig. 7A is drawn to scale and is not a simplified drawing. The present application teaches that a conventional method such as Goto's (in which a silicidation reaction is not source limited) would result in salicide crawl, and that such salicide crawl could be significantly reduced if the inventive method (in which the salicide-forming reaction is source limited) were performed rather than the conventional method. Since there is excess metal available during Goto's silicidation reaction and no metal removal (before the silicidation reaction) from over structures which are to be metal salicide exclusion regions, Goto's method would result in salicide crawl beyond the portions of a MOS transistor structure where metal salicide regions are to be formed.

There is no suggestion in either Goto or Hsu to control thickness of a deposited metal layer to form metal salicide regions in a source limited manner or to limit salicide crawl beyond the portions of a MOS transistor structure where metal salicide regions are to be formed. Goto's teaching at col. 10, lines 50-67 (with reference to Fig. 6A) regarding control of the thickness of a deposited metal layer is merely a teaching that the metal layer thickness affects the sheet resistance of the metal salicide that can be formed by silicidation and subsequent annealing. This teaching does not amount to a teaching or suggestion to modify Hsu's method to reach the invention of claim 1, 8, or 13.

Applicant respectfully contends that there is no teaching determinable from Goto (or other art of record) that Hsu's method should be modified to reach the invention of claim 1, 8, or 13. Absent such teaching determinable from Goto or other specifically identified art of record, Applicant respectfully contends that it is improper to reject claims 1, 8, and 13 on the basis of an unsupported assertion that it would have been obvious to modify Hsu's method to reach the claimed invention. For the foregoing reasons, Applicant respectfully contends that claims 1, 8, and 13 (and all claims depending therefrom) are patentable over Hsu and Goto, whether these references are considered individually or in combination.

Respectfully submitted,
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